

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Greg BENSINGER et al.)
Serial No. TBA)
Filed: July 14, 2004)
For: SYSTEM AND METHOD OF CLOCKING)
AN IP CORE DURING A DEBUGGING)
OPERATION)

Group Art Unit: TBA

Examiner: TBA

Attorney Docket No.: 003921.00204

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office
220 20th Street S.
Customer Window, Mail Stop Amendments
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Sir:

Pursuant to 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §1.97, Applicants submit herewith one Form PTO-1449 identifying information for consideration by the Examiner.

Copies of the documents were provided with the International Search Report for the corresponding PCT application.

If the Patent and Trademark Office determines that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Date: July 14, 2004

By: 

Christopher L. McKee
Registration No. 32,384

CLM/rnn

USPTO Form 1449 Patent and Trademark Office		U.S. Department of Commerce				
INFORMATION DISCLOSURE CITATION Sheet 1 of 1		Attorney Docket No. 003921.00204				
		Serial No. TBA				
		Applicant(s): Greg BENSINGER et al				
		Filing Date: July 14, 2004 10/25/2005	Group: TBA			
U.S. PATENT DOCUMENTS		As per the last 371 req. received in the Office.				
Examiner Initial	Patent No.	Date	Name	Class	Subclass	Filing Date (if appropriate)
FOREIGN PATENT DOCUMENTS						
Examiner Initial	Document No.	Date	Country	Class	Subclass	Translation
						YES NO
	WO 01-20784	22 March 2001	PCT			
	EP 0-685-793	6 December 1995	EUROPE			
	JP 11-259329	24 Sept. 1999	JAPAN			
OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)						
	KOCH G ET AL: " Co-emulation and debugging of HW/SW-Systems" SYSTEM SYNTHESIS, 1997. PROCEEDINGS TENTH INTERNATIONAL SYMPOSIUM ON ANTWERP BELGIUM 17-19 SEPT. 1997, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 17 September 1997, pages 120-125, XP010245612 ISBN: 0-8186-7949-2					
	SUNGJOO YOO ET AL: :Fast Hardware-Software Coverification by Optimistic Execution of Real Processor PROCEEDINGS OF THE CONFERENCE ON DESIGN, AUTOMATION AND TEST IN EUROPE, January 2000, XP010377534					
	PATENT ABSTRACT OF JAPAN Vol. 1999, No. 14, 22 December 1999					
EXAMINER /John J. Tabone Jr./ (02/04/2009)				DATE CONSIDERED		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.						